photoresist remains in place for the protection of the bottom surface of opening 32.

IN THE CLAIMS

Please amend the claims as follows.

1. (Amended) A method of forming a dual damascene structure for copper dual damascene processes, comprising the steps of:

providing a substrate, said substrate having been provided with semiconductor devices structures in or on the surface thereof, at least one point of electrical contact having been provided in the surface of said substrate, a layer of Inter Metal Dielectric (IMD) having been deposited over the surface of said substrate, at least one opening having been created through said layer of IMD, said at least one opening being aligned with said at least one point of electrical contact having been provided in the surface of said substrate;

depositing a layer of first material over the surface of said layer of IMD, filling said at least one opening created through said layer of IMD;

removing said layer of first material from the surface of said layer of IMD, thereby partially removing said first material from said at least one opening created through said

layer of IMD, creating at least one partial opening through said layer of IMD;

baking said substrate for a period of time by applying an elevated temperature in a gaseous environment and under a pressure to said substrate;

depositing a layer of second material over the surface of said layer of IMD, thereby filling said at least one partial opening created through said layer of IMD; and

patterning and etching said layer of second material, creating an opening through said layer of second material that aligns with said at least one partial opening created through said layer of IMD, removing said layer of second material from said at least one partial opening created through said layer of IMD.

2. (Amended) The method of claim 1, said first material comprising I-line photoresist.

3. (Amended) The method of claim 1, said second material comprising DUV photoresist.

13. (Amended) The method of claim 1, with additional steps being performed after said patterning and etching said second layer of material, said additional steps comprising:

depositing a layer of copper over the surface of said second layer of material, thereby filling said opening created through said second layer of material that aligns with said at least one partial opening created through said layer of IMD, thereby further filling said at least one partial opening created through said layer of IMD; and

removing said deposited layer of copper from the surface of said layer of second material.

14. (Amended) The method of claim 13, said step of removing said deposited layer of copper from the surface of said layer of second material comprising steps of copper etch.

15. (Amended) The method of claim 13, said step of removing said deposited layer of copper from the surface of said layer of second material comprising steps of Chemical Mechanical Polishing.

35. (Amended) The method of claim 33, said step of removing said deposited layer of copper from the surface of said second layer of dielectric comprising steps of Chemical Mechanical Polishing.

REMARKS

Examiner Kin-Chan Chen is thanked for thoroughly reviewing the instant application and for examining the Prior Art.

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested.

Claim Objections

Reconsideration of the objections to the claims is respectfully requested based on the following.

The term "CMP" has been removed from claims 15 and 35.

In light of the foregoing response, applicant respectfully requests that the Examiner's objections to the claims be withdrawn.

Claim Rejections

Reconsideration of the claim rejections is respectfully requested based on the following.

The terms "first semiconductor material" and "second semiconductor material" have been amended by removing the term "semiconductor" from these terms, amending these terms to now read as "first material" and "second material". All affected dependent claims have been accordingly amended to avoid problems of lack of antecedent.

In light of the foregoing response, applicant respectfully requests that the Examiner's claim objections be withdrawn.

Claim rejections - 35 U.S.C. § 103(a)

Reconsideration of the rejection of claims 1-12, 17-32 and 37 under 35 U.S.C 103(a) as being unpatentable over Harada et al. (U.S. Patent 6,251,774 B1) is respectfully requested based on the following.

Harada et al. provides for a method of manufacturing a semiconductor device, more specifically Harada et al. provides for:

- a first silicon nitride film
- a first silicon oxide film
- a second silicon nitride film
- a second silicon oxide film

- a via hole is formed through the second silicon oxide film and the second silicon nitride film, exposing an underlying lower wiring layer to which conductive contact is to be established

- a photoresist is embedded into the via hole so as to cover the internal wall of the via hole

- selective removal of the first silicon oxide film and the first silicon nitride film to form a wiring trench.

Harada et al. provides a total of ten embodiments of the invention, since these embodiments use the first embodiment of the invention as the basis and since this basic first embodiment of the invention provided by Harada et al. can be used to show the differences between the instant claimed invention and the Harada et al. invention, applicant will respectfully limit the comparison between the two inventions to comparing the first embodiment of the Harada et al. invention with the instant claimed invention. This limitation does not, in Applicant's considered opinion, diminish in any way the validity of the comparison between Harada et al. and the instant claimed invention since the remaining nine embodiments of the Harada et al. invention also do not provide for the identified differences between the instant claimed invention and the Harada et al. invention as highlighted following.

More specifically, using the first embodiment drawings Figs. 1a through 1f as the basis for comparison, Harada et al. provides for:

Fig. 1A:

- a lower wring layer 30
- a first silicon nitride layer 32 over the layer 30
- a first silicon oxide layer 34 over the layer 32
- a second silicon nitride layer 36 over the layer 34
- a second silicon oxide layer 38 over the layer 36

Fig. 1B:

- a first layer 40 of BARC over layer 38
- a first P.R. mask 42 over the layer 40, opening 44 is created through P.R. mask 42

Fig. 1C:

- a via hole 46 is etched through layer 40, 38, 36, 34, stopping on layer 32

Fig. 1D:

- the first P.R. mask 42 is removed
- opening 46 is filled with a P.R. 48 up to at least the second nitride film 36
- the P.R. 48 is exposed to DUV radiation, hardening the P.R. layer 48

- a second layer 50 of BARC is applied over second silicon nitride film 38 and the hardened layer 48 of P.R.

Fig. 1E:

- a second P.R. mask 52 is formed, creating opening 54 therethrough that is aligned with opening 44 of the first P.R. mask

Fig. 1F:

- layers 50, 38, 36, 34 and 32 are dry etched in accordance with the opening 54 created through the second P.R. mask, creating an opening 56 having the profile of a dual damascene opening.

As stated supra, the additional embodiments of the Harada et al. invention provide variations on the first embodiment of the invention. For instance, the second embodiment of the Harada et al. invention, as shown in Figs. 2a through 2e, does not apply layer 48 (Fig. 1d) as is apparent from Fig. 2d.

The third embodiment of the Harada et al. invention, as shown in Figs. 3a through 3f, uses a BARC layer 50 (see Fig. 3D) which is embedded throughout the inside of the via hole 46.

The remaining embodiments of the Harada et al. invention show similar variations on the first embodiment of the invention, for all of these variations the Harada et al. invention does not address a concern of creating damascene

interconnects, as states in the specification of the claimed invention, that is, see page 18 of the specification of the invention, as follows:

It is clear from the cross section that is shown in Fig. 2e that the opening 30 that is created through layer 28, which aligns with the opening 24 created through layer 22 (Fig. 2c), creates a combined opening that has the cross section of a dual damascene structure. **Inhibiting however** the creation of a dual damascene structure of desired performance characteristics of resistivity, reliability, adhesion to surrounding layers of dielectric and the like is the layer 29 of photoresist scum that remains in place overlying layer 26. This layer is formed as a consequence of processing conditions that have previously been highlighted, among these reasons incomplete reaction of the etch of the layer 28 of DUV photoresist and, further, due to adsorption or intrusion of moisture by the reacted DUV photoresist 26. The moisture, which plays a role in this process of forming scum layer 29 of photoresist, originates from the layer 22 of IMD. This formation of a layer 29 of scum photoresist has been observed to be dependent on the dielectric constant of the layer 22 of IMD, with an increase in the formation of this layer 29 taking place for low-k, non-oxide containing dielectric material.

It is clear and has previously been highlighted that the formation of layer 29 must be prevented. The claimed invention provides, for this purpose, a processing step that is performed after the completion of the structure that is shown in cross section in Fig. 2c, that is after the I-line layer of photoresist has been etched back and a significant portion of the sidewalls of opening 24, Fig. 2c, is exposed.

The specification continues this explanation, an explanation this is reflected in the claims of the invention. For instance claim 1, which specifies a method of forming a dual damascene structure for copper dual damascene processes, and from which is quoted following with underlined aspects of the instant claimed invention which are not provided by the Harada et al. invention: baking said substrate for a period of time by applying an elevated temperature in a gaseous environment and under a pressure to said substrate.

This step of baking, provides for, as quoted from page 19 of the specification:

At that time, that is after the processing step that results in the cross section shown in Fig. 2c and before the processing step of Fig. 2d of depositing layer of DUV

photoresist, a baking step is added to the processing cycle. This baking step removes moisture from the layer 26 of IMD so that this moisture is no longer present during the step of etching the layer 26 of DUV photoresist, thus removing a key contributor to the formation of scum photoresist layer 29 of Fig. 2e.

Dependent claims 2, 3, 20 and 23 specify the first material comprising I-line photoresist and the second material comprising DUV photoresist. These particular materials have shown to provide optimum results, as has been explained in detail in the specification using for this purpose Figs. 2d-2e.

The claimed invention provides for the creation of an optimum opening that can be used for the creation of damascene and dual damascene interconnects. The claimed invention, for this reason, provides for the prevention of the occurrence of scum 29, shown I cross section in Fig. 2e of the instant claimed invention. Since the photoresist and the development there-of is a major contributor to the occurrence of scum 29, it stands to reason that the contributors (to the scum formation) must be limited in their effect, a limitation that is provided by selecting particular types of photoresist as specified in dependent claims 2, 3, 20 and 23.

Regarding claims 4, 5, 24 and 25, it must be stated that, when specifying a new and innovative processing step that is provided for a more complicated processing sequence, it is required that specifics are provided as to how the new and innovative processing step can optimally be performed.

Dependent claims 2, 3, 20 and 23 provide this required detail by specifying that the baking of the substrate can be performed using a hot plate or can be performed inside a high-temperature furnace. Without these claims the claimed invention would be incompletely specified and would therefore be open to ambiguous and unclear interpretation.

Claims 6-8, 12, 26-28 and 32 provide further detail for the baking of the substrate. These processing conditions apply most favorably for the objective of the claimed invention, which is to remove photoresist scum from openings that have been created using a layer of photoresist.

The question can be asked if, without the detail and limitations that are provided by claims 6-8, 12, 26-28 and 32, the claimed invention would be completely specified. The answer to this question would be that this would not be the case and that therefore for instance any temperature or any pressure or

any length of baking time would be acceptable to achieve the objectives of the instant claimed invention.

This latter supposition obviously cannot be sustained, one would for instance not want to expose a substrate to elevated temperatures for a period of over a year, or over two years, etc. These conditions must therefore be limited, a limitation that is provided by claims 6-8, 12, 26-28 and 32.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 1-12, 17-32 and 37 under 35 U.S.C 103(a), be withdrawn.

Claim rejections - 35 U.S.C. § 103(a)

Reconsideration of the rejection of claims 13-16 and 33-36 under 35 U.S.C 103(a) as being unpatentable over Harada et al. (U.S. Patent 6,251,774) as applied to claims 1-12, 17-32 and 37 above and further in view of Chooi et al. (U.S. Patent 6,284,657 B1) or Chung et al. (U.S. Patent 6,017,817) is respectfully requested based on the following.

The relative merits of Harada et al. with respect to the instant claimed invention have been highlighted supra and are

enclosed at this time by reference as being equally applicable to claims 13-16 and 33-36.

Chung et al. and Chooi et al. provide for fabricating dual damascene interconnects using steps of depositing layers of semiconductor material, patterning these layers and filling the created pattern with interconnect metal.

Chung et al. and Chooi et al. however also do not provide for removing moisture from a layer of dielectric that is used for creating interconnect patterns there-in and therefore do not provide for the critical step of baking that is provided by the instant claimed invention, as detailed above and being enclosed as this time by reference as equally being applicable to the Chung et al. and the Chooi et al. inventions as these inventions relate to the instant claimed invention.

Dependent claims 13-16 and 33-36 provide further detail as to how the damascene structure of the claimed invention can be completed and the materials that are preferably used for such a completion as provided by the instant claimed invention.

Without these specifications, the instant claimed invention would provide for and specify only a partial process, which in

and of itself would be without meaning, since such a process would not create a useful semiconductor entity.

The claims 13-16 and 33-36 complete the damascene process by specifying filling the created opening, having no scum residue due to the instant claimed invention, with copper and using a low-k dielectric for the creation of the damascene openings since this type of dielectric is known to have a relatively high moisture content and therefore benefits most from the processing steps of the claimed invention.

While applicant acknowledges the teachings of Harada et al., Chung et al. and Chooi et al. as cited by the Examiner, and although applicant does not necessarily agree that the Examiner's arguments show sufficient and proper basis for suggestion or motivation to modify or combine Harada et al. with Chung et al. and Chooi et al., applicant nonetheless also asserts that there is absent within the portions of Harada et al., Chung et al. and Chooi et al. or any combination thereof, as cited by the Examiner, an express or inherent teaching of each and every limitation within applicant's claimed invention as taught and claimed within amended claims of the claimed invention.

In this regard, applicant claims that there is absent form the portions Harada et al., Chung et al. and Chooi et al. or any combination thereof, as cited by Examiner, a teaching of creating an opening through a layer of dielectric such that the formation of scum is prevented.

This latter aspect of the claimed invention is specified in the above quoted independent claim 1 as well as in independent claim 18, which specifies a method of forming a dual damascene structure for copper dual damascene processes, as highlighted following:

- providing a substrate
- depositing a first layer of dielectric over the surface of the substrate
- creating at least one first opening through the first layer of dielectric
- creating a layer of protective material over a bottom surface of the at least one first opening
- baking the substrate, including the first layer of dielectric and the layer of protective material
- depositing a second layer of dielectric over the surface of the first layer of dielectric, and

- creating at least one second opening through the second layer of dielectric, the at least one second opening being aligned with the at least one first opening.

Conventional processing for the creation of an opening through a layer of dielectric are subject to subsequent depositions of conductive material, which are required to create a conductive plug in the opening, which will not result in a uniform deposition of the conductive material throughout the cross section of the created opening. The conductive material will, due to the presence of a layer of scum, be prevented from being deposited over the bottom and the lower extremities of the sidewalls of the created opening, thus being prevented from forming an interface with the underlying surface. Conductive contact between the plug that fills the opening and an underlying point of electrical contact can therefore not be established such that this contact is of low resistivity and high reliability. In order to meet these latter objectives, the claimed invention prevents the formation of scum.

It would not be obvious to combine the teachings Harada et al., Chung et al. and Chooi et al., since there is no suggestion or motivation in the teachings of any of the patents of the present claimed invention.

Contrary to the Examiner's assertion that of Harada et al., Chung et al. and Chooi et al. discloses forming a scum-free opening through a layer of dielectric, of Harada et al., Chung et al. and Chooi et al. do not mention the removal of moisture from the layer of dielectric as part of the processing sequence of forming a damascene interconnect through-in and there-through.

None of the applied or known references address the claimed invention as shown in the amended claims in which the effects of moisture content in surrounding layers of dielectric are neutralized by removing the moisture from the layers of dielectric prior to completion of the opening that is created through the layers of dielectric. The claimed invention is believed to be patentable over the prior art cited, as it is respectfully suggested that the combination of these various references cannot be made without reference to Applicant's own claimed invention.

None of the applied references address the problem of creating a damascene contact plug having low resistivity, high reliability and high adhesion to surrounding layers of dielectric. Applicant has claimed the process in detail. The processes of Figs. 2a-2g are both believed to be novel and

patentable over these various references, because there is not sufficient basis for concluding that the combination of claimed elements would have been obvious to one skilled in the art.

That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is desirable. We believe that there is no such basis for the combination. We therefore request Examiner Kin Chan Chen to reconsider the rejection in view of these arguments and the amendments to the Claims.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 13-16 and 33-36 under 35 U.S.C 103(a), be withdrawn.

The prior art made of record and not relied upon that is considered pertinent to Applicant's disclosure, that is Chang et al. (U.S. Patent 6,319,809 B1), Lin et al. (U.S. Patent 6,042,999) and Chang (U.S. Patent 5,643,407) have been examined and have been found to be of general interest to the claimed invention.